WHAT IS CLAIMED IS:

1. A keyed clamp circuit comprising:

a clamp circuit clamping a video signal including an equalizing pulse and a vertical synchronization signal based on a clamp pulse;

a synchronization signal separation circuit separating a synchronization signal from the video signal clamped by the clamp circuit; and

a clamp pulse generation circuit generating the clamp pulse for the clamp circuit so that a pulse width of the clamp pulse is shorter, during an equalizing pulse period, than a vertical synchronization signal period, based on the synchronization signal from the synchronization signal separation circuit.

2. A keyed clamp circuit comprising:

a clamp circuit clamping a video signal including an equalizing pulse based on a clamp pulse;

a synchronization signal separation circuit separating a synchronization signal from the video signal clamped by the clamp circuit; and

a clamp pulse generation circuit generating the clamp pulse for the clamp circuit so that a pulse width of the clamp pulse is shorter than a pulse width of the equalizing pulse during an equalizing pulse period, based on the synchronization signal from the synchronization signal separation circuit.

3. The keyed clamp circuit of claim 2, wherein the clamp pulse generation circuit comprises a capacitor, a charging circuit charging the capacitor based on the synchronization signal from the synchronization signal separation circuit and a discharging circuit discharging the capacitor and a comparator comparing a charging voltage of the capacitor with a reference voltage.

4. The keyed clamp circuit of claim 3, wherein a current ratio of the charging circuit to the discharging circuit is set to generate the clamp pulse for the clamp circuit.

5. A keyed clamp circuit comprising:

a clamp circuit clamping a video signal including an equalizing pulse and a vertical synchronization signal based on a clamp pulse;

a synchronization signal separation circuit separating a synchronization signal from the video signal clamped by the clamp circuit;

a clamp pulse generation circuit generating a clamp pulse for the clamp circuit so that a pulse width of the clamp pulse during a vertical synchronization signal period is longer than the pulse width of the clamp pulse during an equalizing pulse period, based on the synchronization signal from the synchronization signal separation circuit.

6. The keyed clamp circuit of claim 5, wherein the clamp pulse generation circuit comprises a capacitor, a charging circuit charging the capacitor based on the synchronization signal from the synchronization signal separation circuit and a discharging circuit discharging the capacitor and a comparator comparing a charging voltage of the capacitor with a reference voltage.

7. The keyed clamp circuit of claim 6, wherein a current ratio of the charging circuit to the discharging circuit is set to generate the clamp pulse for the clamp circuit.

8. The keyed clamp circuit of claim 6, wherein a current ratio of the charging circuit to the discharging circuit is set according to the vertical synchronization signal.

9. The keyed clamp circuit of claim 6, wherein the clamp pulse generation circuit further comprises a constant current source turning on and off based on the vertical synchronization signal.

10. The keyed clamp circuit of claim 6, wherein the clamp pulse generation circuit further comprises a switch opening and closing based on the vertical synchronization signal and a constant current source turning on and off based on the opening and closing of the switch.

11. The keyed clamp circuit of claim 6, wherein a voltage of the comparator changes

based on the synchronization signal from the synchronization signal separation circuit.